analog voltage to generate different colors. A flat panel display subsystem is completely digital. It gen[illegible]s colors (and gray scales) by varying th[illegible]mber of red, green, or blue (or monochrome) pixels that are refreshed over a series of frames. This technique is

video subsystem. While multimedia applications for portable computers are very limited to date, many of the ideal applications for multimedia computing will require portability. For instance, presentations with live video will most effectively communicate

scales and formats the video information and stores the [illegible] in a separate frame-store. The fram[illegible]e interfaces directly to the RGB pixel port on the flat panel controller. A color-key signal is passed between the

Designing A Digitally Programmable, Loop-Powered 4-20mA Controller

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The accompanying schematic shows an isolated 4-to-20mA current loop controller in which a digital-to-analog converter (DAC) sets the amount of current that flows through the loop. Power for the controller circuit is derived from the loop power, with the circuit working over a loop voltage range from 8V to 36V. Since the controller is intended to be isolated, all control signals must be opto-isolated before being applied to the DAC. To limit the number of opto-isolators required, a serial-loading DAC is preferable.

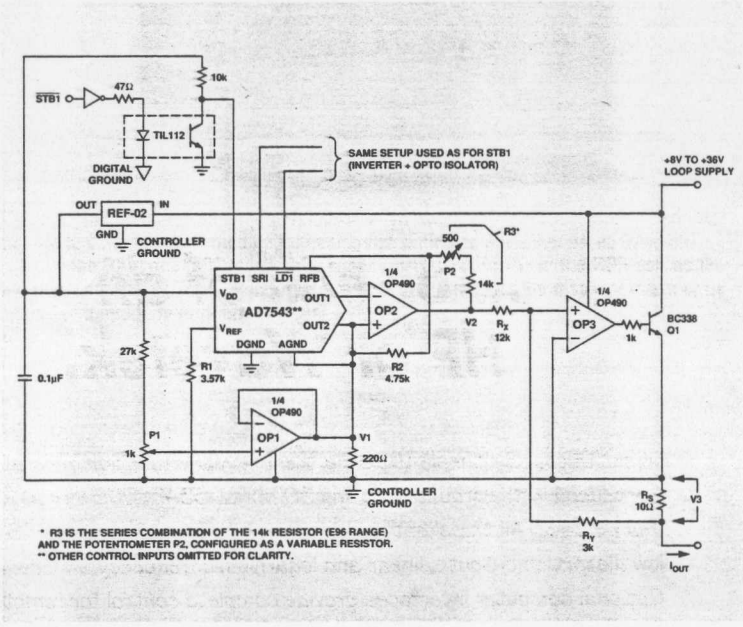
The AD7543 from Analog Devices is a serial loading, 12-bit DAC which can be loaded and controlled with only three lines: STB1, SRI and LD1. Since the opto-isolators act as signal inverters, the microcontroller, PC or whatever is supplying the control signals must take this into account and generate the appropriate waveforms for the opto-isolators. The serial data is clocked into the input register on the rising edge of STB1. Data is loaded with the MSB as the first bit in the data stream. Once the new data word has been clocked in, it is transferred to the DAC register by taking LD1 low momentarily.

The DAC output voltage at V_2 is given by the equation

$$V_2 = V_1 + V_1D(1 + R3/R2)$$

where D is the fractional equivalent of the DAC digital input code in decimal form and can vary from 0 to almost unity (4095/4096). This output voltage is transformed into a loop current by means of OP3 and Q1. OP3 drives the NPN transistor Q1, configured as an emitter follower in the feedback loop, to maintain a current necessary to keep the voltage V_3 across R_S, the sense resistor, equal to the voltage across R_Y, the feedback resistor. Since the ratio of R_X to R_Y is 4, the ratio of voltages across R_X and R_Y must be the same, i.e.

$$V_3 = V_2/4$$



Schematic for a 4 to 20 mA current loop controller. The digital code to the DAC sets the amount of current that flows in the loop.

Thus V_3, and ultimately the loop current, follows the DAC output voltage V_2. In order to operate off of low loop voltages, the voltage V_3 should be as small as practical. With the 10Ω used for R_S in Figure 1, V_3 varies from approximately 40mV (at 4mA loop current) to approximately 200mV (at 20mA loop current).

From the first equation, with all 0s in the DAC,

$$V_2 = V_1$$

and with 1s in the DAC and $(1 + R_3/R_2) = 4$,

$$V_2 \approx 5V_1$$

Thus, as the loop current changes from 4mA to approximately 20mA, V_2 changes from V_1 to approximately $5V_1$ and, because of the x4 attenuation due to the R_X/R_Y ratio, the sense voltage V_3 correspondingly changes from $V_1/4$ to $5V_1/4$.

The zero-scale loop current is calibrated by adjusting potentiometer P1, with all 0s in the DAC, until a current of 4mA is measured flowing in the loop. The full-scale loop current is calibrated by adjusting potentiometer P2, with all 1s in the DAC, until a current of 20mA – 1 LSB is measured flowing in the loop. One LSB of current is equal to 16/4096mA or 3.9 μA. The zero-scale adjustment is unaffected by the full-scale adjustment.

Resistor R1 is chosen to be equal to the parallel combination of resistors R2 and R3. This avoids the absolute value of the DAC ladder from appearing in the output expression for V_2 (assuming $R_{FB} = R_{LAD}$, i.e. no DAC gain error). Ideally, resistors R1, R2 and R3 should be the same type and from the same manufacturer to ensure that their TCs match and track each other. However, since it is necessary to provide full-scale adjustment, R_3 consists of a fixed 14kΩ metal film resistor and a 500Ω 10-turn potentiometer P2. Although the TCs of the potentiometer and the metal film resistor will almost certainly not match, the additional drift will not be significant since the TC of the much larger fixed resistor will dominate.

The 220Ω resistor on the output of OP1 acts as a pull-down resistor and helps to keep the voltage V1 constant as the DAC digital input code changes. The actual loop current that flows is given by:

$$I_{out} = V3(1/R_S + 1/R_Y)$$

R_S is set to 10Ω and R_Y is set to 3 kΩ. With 4 mA flowing (I_{out} = 4 mA), using the above equation we see that V3 = 39.867 mV (V2 = 159.468 mV). From the first equation, we know that V2 = V1 at the all 0s code. This voltage, as mentioned above, is set by P1.

At full-scale (I_{out} = 20mA – 3.9μA), using the above equation we see that V3 = 199.336 mV (V2 = 797.344 mV). This voltage is set by P2.

The circuit will actually work with a loop voltage as low as 5V but the accuracy will be reduced to 9-bits. In such a situation, the REF-02 is replaced with an LM334 constant current source (RSET = 22Ω) driving a 3.3V Zener diode. The reduced V_{DD} voltage on the DAC accounts for the degraded linearity.

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